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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/785,006	02/16/2001	Aaron Schoenfeld	303.259US3	5063

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EXAMINER	
PERT, EVAN T	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 07/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H:A

Office Action Summary	Application No.	Applicant(s)	
	09/785,006	SCHOENFELD, AARON	
	Examiner	Art Unit	
	Evan Pert	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-25,35-39 and 41-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-25,35-39 and 41-43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 17 and 39 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim.

Claims 17 and 39 recite a "polished" limitation that is already included in the independent claims such that dependent claims 17 and 39 do not further limit subject matter of a previous claim.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 11-25, 35-39, and 41-43 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Indefinite – "polished"

All of the claims include the limitation that a side surface of a semiconductor die is "polished." However, the term "polished" in claims 11, 14, 15, 17, 18, 19, 22, 25, 35, 39 and 41 is a relative term, which renders the pending claims indefinite. The term "polished" is not defined by the claims, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not reasonably understand the scope of the claimed invention.

For purposes of examination, any semiconductor die that has "a high quality side face surface which does not need polishing" is considered to fall within the scope of a semiconductor die that has a "polished side surface."

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 11-16, 18-25, 35-38, and 41-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over EP 0 678 904 A1 (Boruta) in view of US 5,408,739 (Altavela et al.) with US 4,804,641 (Arlt et al.).

Species I = "Semiconductor die" having "stepped edge" (i.e. "bi-level edge")

[e.g. claims 18-25, 35-39 and 41-43 are "readable on" Species I].

Species II = "Semiconductor die" having "planar perimeter side surfaces" that *inherently* extend between major faces of the semiconductor die.

[e.g. claims 11-17 are "readable on" Species II].

The primary reference to Boruta discloses semiconductor die that have active circuitry on a first planar surface opposite a second planar surface (i.e. active circuitry on the side with test circuitry in the dicing lanes), with side surfaces having bi-level (comparing Species I to Fig 2D of Boruta) and flat (comparing Species II to Fig. 1B of Boruta) configurations, meeting the wordy limitations drawn to *relative orientation* of "surfaces" of semiconductor die with bi-level (i.e. claims 18, 20-25, 35, 36, 38, 41 and 43) and flat (i.e. claims 11, 12, 15, 16) side surfaces.

Boruta does not disclose an unused buffer area region around active circuitry on the semiconductor die, wherein the region is specifically "disposed within approximately 5 microns of an edge of the active region," or that side surfaces of diced die according to their invention are "polished" surfaces. However:

The Arlt et al. reference (US 4,804,641) discloses a problem known for the dicing of the Boruta reference in that "chippage" occurs at the cut edges from sawing [col. 1]. As explained by the Arlt et al. reference,

> In the miniaturization of semiconductor components, it is important to save space and therefore the space on the surface of a semiconductor wafer should be utilized to the fullest extent. Consequently, the present invention seeks to reduce the width of the sawing track without reducing the quality or yield of the individual chips obtained from a semiconductor wafer by sawing [col. 1, lines 40-46].

To achieve the reduction in the sawing track, a narrow buffer region "of about 5 microns" is located around the active circuitry of a die, before cutting, and:

> Due to the presence of the chippage stoppage border 1, the width of the saw track in the sawing region 7 can be reduced in size without reducing the quality or yield of individual semiconductor components. In this way, costly space on the semiconductor wafer can be saved and more semiconductor components can be manufactured per semiconductor wafer as a result [col. 3, lines 7-13].

It would have been obvious to one of ordinary skill in the art at the time of the claimed invention to adopt the dicing improvement of the Arlt et al. reference for practicing the dicing method of Boruta. One of ordinary skill in the art would have been motivated to adopt the dicing method improvement of the Arlt et al. reference for practicing the method of Boruta because, for example, "space of the semiconductor wafer can be saved," as explained by the Arlt et al. reference.

Regarding claims 13, 19, 37 and 42, each of the die are rectangular, as is known in the art, because the scribe lines are conventionally perpendicular (such as shown by the cover Figure of the Arlt et al. reference).

While the Boruta reference does not teach that side surfaces of the cut die are "polished," applicant's term "polished" is indefinite per the rejection under 35 USC 112, set forth above (i.e. "polished" not being *quantified*), such that a side surface that "does not need polishing" in the prior art is substantially already "polished."

The Arlt et al. reference explains that extent of chippage at edges of a cut die:

> depends on various sawing parameters such as quality of the saw blade, the age of the saw blade, the sawing rate, and the like. The chippage is also dependent upon parameters of the semiconductor wafers such as, for example, the doping of the semiconductor wafer in the sawing region, the type and number of surface layers, and similar factors [col. 1, lines 11-25].

Altavela et al. (US 5,408,739) discloses that a "dicing cut" made with "a resin blade" is "well known in the art of semiconductor dicing and can provide a very high quality [side] surface 90 which does not need further processing, such as polishing" [col. 6, lines 55-65].

Thus, the Altavela et al. references discloses that a "resin blade" gives a high quality cut that results in a surface that is indistinguishable from an ambiguously claimed "polished surface" because a cut surface from a "resin blade" does "not need to be polished."

It would have been obvious to one of ordinary skill in the art at the time of the claimed invention to adopt "resin blades," for practicing the dicing method of Boruta, since the blades give a high quality "polished" cut, as known in the art per Altavela et al.. One of ordinary skill in the art of semiconductor dicing would have been motivated to use a "resin blade," because a resin blade results in "a very high quality" side surface with "does not need to be polished." Since the side surfaces of the die do "not need to be polished," they are necessarily indistinguishable from applicant's ambiguously claimed "polished" sides [see rejection under 35 USC 112 above].

In summary, applicant's claimed invention is not patentable under 35 USC 103(a) in view of the combination of Boruta, Altavela et al. and Arlt et al., wherein it would have been obvious to one of ordinary skill in the art at the time the claimed invention was made, to adopt the technique to avoid chippage when dicing as taught by Arlt et al. in the dicing technique of Boruta that removes test structures from the dicing lanes, using a high quality resin blade that gives a high quality edge surface that can be considered "polished."

One of ordinary skill in the art would have been motivated to adopt the technique of Arlt et al. that leaves a buffer of about 5 microns around the active circuitry of the chip, in order to "save space," and would be motivated to adopt a resin blade that gives a polished cut per the Altavela et al. reference, to minimize the chippage in Arlt et al. that could encroach the active circuitry inside the unused buffer region surrounding the active circuitry.

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Evan Pert whose telephone number is 571-272-1969. The examiner can normally be reached on M-F (7:30AM-3:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EVAN PERT
PRIMARY EXAMINER

ETP
July 18, 2005